A Flexible Multiband Reconfigurable Receiver for Wireless Endoscopic Capsule Streaming Video

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***Abstract*—An on-the-fly reconfigurable wireless receiver was developed to demodulate high-speed, multi-band modulated signals in the sub-GHz band. The extreme flexibility is enabled by an FPGA as central processing core, reconfigurable at run-time with any demodulation core. The receiver front-end is entirely controllable from a software GUI. The software platform allows high-speed real time transfer of demodulated wireless endoscopic capsule image data from the FPGA through a USB interface IC, for further processing on a PC. A newly developed FSK demodulation core is used as case study for assessing the receiver's quality. The extreme receiver flexibility allows for efficient practical design space exploration in research for the most optimal high-speed communication system for wireless endoscopic capsule links.**

I. Introduction

Wireless capsule endoscopy is getting wider acceptance among specialists as a first examination of the gastro-intestinal (GI) tract, in case of anomalies [1], [2]. For understandable comfort reasons, the barrier for the patient to undergo a GI examination has dropped considerably, increasing the chances of early detection of GI cancers. However, capsule endoscopy does not offer yet a justified alternative for the traditional - wired - endoscopy, on ground of the capsule's limited frame rates, limited image resolution and the lack of active locomotion. A qualitative specification comparison is depicted in table I. The reason for these shortcomings is due to the limited available energy in a battery-powered capsule. Available energy in two button silver-oxide cells is typically 50 mAh, just enough to foresee passive locomotion, a frame rate of a few frames per second and low-resolution pictures [1]. Recently, a new wireless powering technology was developed based on 3-D inductive coupling. It is able to continuously supply up to 300 mW, independent of its orientation, in the same volume as 2 button cells [3]. This development enabled the use of a better and faster image sensor, requiring higher data rates to wirelessly transmit these images through the body. A typical data rate calculation for a wireless endoscopic camera looks as in the example shown in table I. It is clear that when wirelessly transmitting image information through the body, the high information content related to high resolution - high frame rate images, requires a large bandwidth. It is possible to increase the bandwidth efficiency by moving to higher order modulation schemes (QPSK, 8-PSK, OFDM, ...), but these are generally more complex - thus power hungry to implement. Binary shift keying is still the most applied modulation scheme in wireless endoscopy applications [4]. When opting for frequency shift keying (FSK) modulation, simple to implement and widely used because of its high robustness against noise, the required spectral bandwidth for transmitting raw image data can be estimated through Carson's rule [5]. The bandwidth required by a frequency modulated signal occupies at least twice the highest modulating frequency. Applied on the figures of table I, the transmitting antenna, receiving antenna and receiver require a bandwidth of at least 4 MHz. Higher image resolution, higher frame rate, error correction or reduced compression demand an even larger bandwidth. FSK modulation at high data rates rules out the use of industrially and governmentally accepted bands, like Medical Implant Communication Services (MICS) [6] between 402 and 405 MHz (10 bands of 300kHz), and Industrial, Scientific and Medical band (ISM f1) between 433.05 and 434.79 MHz (1.74 MHz bandwidth) [7]. Furthermore, the ISM band does not allow the transmission of streaming video.

The selection of the most optimal carrier frequency for transmission of information through the human body is a tedious trade-off, discussed in [4]. Literature suggests carrier

	Traditional endoscopy	Wireless endoscopy
resolution	1280×1000	256×256 px
framerate	20–30	2–7 fps
steering	active	passive
range	upper and lower GI	full GI

TABLE I
QUALITATIVE COMPARISON BETWEEN TRADITIONAL AND WIRELESS ENDOSCOPY

FR (framerate)	:	15 fps
R (resolution)	:	640×480 px
PD (pixel depth)	:	10 bit/px
CR (compression ratio)	:	25
DR (data rate)	: $\frac{(FR \times R \times PD)}{CR} = 1.843$ Mbps	

TABLE II
DATA RATE CALCULATION EXAMPLE FOR A TYPICAL WIRELESS ENDOSCOPY APPLICATION.

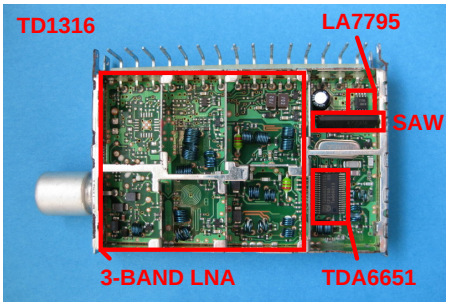
frequencies below 1 GHz, as lower frequencies are absorbed less by human tissue. Less transmission power is required as such, to transmit electro-magnetic (EM) waves through the body [8]. On the other hand, only a small volume is available for housing the transmitting antenna inside the swallowable capsule, typically $\lambda/300 \ldots \lambda/50$ in size. This leads to very inefficient antennas, as the antenna losses (skin effect and ohmic resistance) become much larger than the radiation resistance - being the equivalent resistance part of the power that is actually converted into radiation. This inefficiency requires more power to be delivered to the transmitter antenna to obtain a certain range. The bandwidth limit of electrically small antennas poses an additional design hurdle, making it difficult to design a small-sized wideband antenna at low ($<$ 1GHz) frequencies [9], [10]. Because of the short range ($<$ 1 m) between the transmitter and receiver and the inferior radiation properties of the antenna, it is expected that more efficient wireless links can be achieved by using near-field inductive transmission. On the other hand, there exist virtually no constraints for the receiver design : the available energy to power a low-noise, wide-bandwidth receiver is unlimited, and there is almost no area constraint for the receiving antennas. In this view, as much processing as possible (both analog and digital) should be shifted towards the receiver, to reduce the power consumption of the transmitter to an absolute minimum. Previous work [4] describes a custom designed FSK transmitter based on a free-running Colpitts voltage controlled oscillator (VCO). The receiver, based on the SA639 FSK demodulator IC of NXP, requires a separate low-noise amplifier (LNA) and local oscillator (LO). Although working adequately, this receiver setup was used at its bandwidth limits, and did not provide the flexibility to move to other frequency bands or demodulate alternative modulation schemes.

The requirement for larger bandwidths and uncertainty about the final carrier frequency push us towards a more flexible receiver solution. This enables the use of larger bandwidths, more complex modulation schemes and the flexibility to choose the carrier frequency in a wide range in the sub 1 GHz band. As no commercially available multi-modulation high data rate receiver solutions exist in the sub-1GHz band, a custom flexible multiband reconfigurable receiver was built and tested. The design of the receiver is described in section II, the user interface is discussed in section III and a case study is described in section IV.

II. Receiver Design

A. Specifications

In the original FSK transmitter design [4], the carrier frequency of 144 MHz is a compromise between antenna efficiency and electromagnetic (EM) wave attenuation. The new receiver design has been expanded with the option to investigate the transmission efficiency at lower and higher frequencies, and its influence on wireless link efficiency. Carrier frequencies below 70 MHz enable the use of high-speed ferrites in the antennas, increasing the coupling between the transmission and reception antennas. Frequencies above



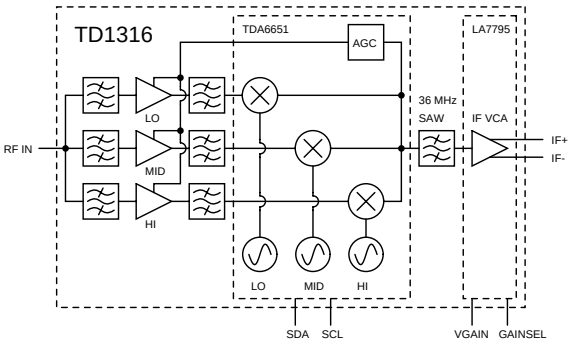


Fig. 1. Photograph and block diagram of the TD1316 DVB-T frontend

400 MHz allow the application of off-the-shelve chip antennas, considerably reducing the overall design effort. The tuning frequency range is therefore set between 50 and 500 MHz.

As explained in the introduction, the required bandwidth for FSK modulated wireless capsule streaming video is minimally 4 MHz, automatically following as the minimal bandwidth of the receiver. For the current transmitter design, FSK demodulation is required, but future firmware updates will enable demodulation of other more bandwidth efficient schemes like differential phase shift keying (DPSK), M-ary PSK (QPSK,8PSK,...) or orthogonal frequency division multiplexing (OFDM), without any hardware change. This flexibility forces part of the receiver chain to be implemented in a reconfigurable technology, like a field-programmable gate array (FPGA) or digital signal processor (DSP).

B. Design Approach

1) RF Front end: There is no off-the-shelf solution fitting all the design challenges as a whole. A partial solution was found inside a commercial digital video broadcasting terrestrial (DVB-T) receiver. The TD1316 (Figure 1) canned analog front-end from NXP fits the specifications, containing a discrete tri-band LNA, a NXP tri-band TDA6651 demodulator with integrated phase locked loop (PLL), a 32.13-40.13 MHz surface acoustic wave (SAW) intermediate frequency (IF) filter and a Sanyo LA7795 voltage controlled amplifier (VCA) for the IF amplification. The tuning range of the TD1316 is 51–858 MHz, the IF bandwidth is 8 MHz centered around 36.13 MHz and the overall receiver gain is maximally 80 dB. Tuning frequency and AGC settings can be controlled by I^2C bus communication, while the gain of the LA7795

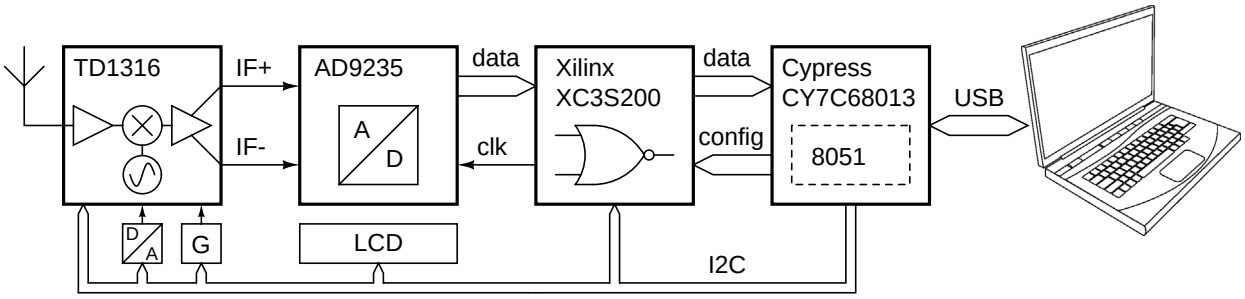


Fig. 2. Complete block diagram of the receiver implementation

IF amplifier can be controlled by an external voltage. The TD1316 module was adapted to increase the overall gain range to 90 dB. The IF VCA is a fully differential amplifier, improving its immunity to common mode disturbances and even-order harmonic distortion.

In the initial receiver design of [4] the FSK demodulation was performed completely analog, while in this design the IF band is immediately digitized, keeping full flexibility over the demodulation process.

2) Analog-to-digital conversion: When digitizing an analog signal, mostly Shannon [11] or beyond Shannon sampling is used to retain all information contained in the original signal band. This requires the sampling frequency to be at least two times the highest frequency of interest, in the IF frequency case 2×40.13 MHz. As all modulated information is contained in a bandwidth of 8 MHz, it makes sense to down-modulate the IF band to the base-band, before sampling it at 16 MHz. Both sampling and downmodulation can be performed in one step by undersampling of the IF band. This generates less data overhead and mixes the sampled band to another band, by aliasing. When carefully selecting the undersampling frequency, the 8 MHz IF band centered around 36.13 MHz can be effectively folded down to the base band. The principle of Shannon versus undersampling is depicted in figure 3, where for clarity the IF band is centered around 36 MHz. When sampling at 16 MHz, the original band between 32 and 40 MHz is folded every 8 MHz ($f_s/2$), resulting in a down-sampled band between 0 and 8 MHz. The SAW filter limits the IF band between 32.13 and 40.13 MHz, while attenuating other frequency components. This largely avoids overlapping of the aliases and folding back of out-of-band noise to the base band. Although the speed requirement for the ADC and the following digital processing is considerably relaxed by the use of undersampling, there is an increased sensitivity to clock jitter, effectively decreasing the signal to noise ratio (SNR) [12]. A fully differential analog to digital converter (ADC) AD9235BRUZ-40 of Analog Devices was selected, with a resolution of 12 bit and maximal conversion speed of 40 MHz. This IC samples the IF band through a transformer connection, and provides a direct parallel output to easily interface with any digital logic, e.g. a DSP or a FPGA.

3) Reconfigurable digital core: The ADC interfaces to a Xilinx Spartan3 XC3S200 FPGA, the central part of a generic

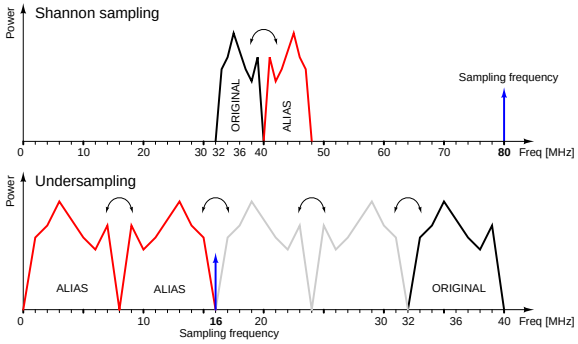


Fig. 3. The principle of Shannon sampling at 80 MHz versus undersampling at 16 MHz, assuming an IF band between 32 and 40 MHz.

USB interface, described in earlier work [13]. The FPGA can be configured through USB, enabling the implementation of virtually any demodulation core without any physical hardware change. The FPGA interfaces with a Cypress high-speed USB interface IC, type CY7C68013A. A free C++ library and Windows driver is available from Cypress to interact with the USB interface chip through software (SuiteUSB), while for Linux the Libusb library can be used. The CY7C68013A contains an on-board 8051 microcontroller core, which is configured at connection with a PC. The 8051 handles basic low-speed functions like configuration of the FPGA and controlling the I^2C bus, using received USB data. High-speed data, e.g. streaming video, is transferred directly from the parallel interface of the FPGA and the CY7C68013A to the configured USB first-in first-out (FIFO) endpoint buffers. This data can be transparently accessed by the PC user software through the Cypress library or Libusb functions, for further processing.

4) Additional hardware: To maximize the flexibility and user control of the receiver board, additional hardware is foreseen, controlled by the generic interface I^2C bus. Two NXP PCA9538 8-bit IO expanders enable the control of the IF VCA coarse gain and a status LCD screen. 7 remaining IOs are available on a patch area, for possible expansion of the board. The fine gain of the IF VCA is controlled by a I^2C 10-bit buffered DAC, the TI DAC6571.

C. Design Result

The full block diagram of the receiver is depicted in figure 2. The board was designed in Cadstar on a two-layer PCB, as an expansion board for the generic USB interface of [13]. Separate voltage regulators and local decoupling for the ADC and IF demodulator ensure limited noise coupling through the supply and ground lines from the generic USB interface. Small 22 Ohm resistors in series with the high-speed data lines from the ADC to the FPGA avoid excessive electromagnetic emission, by limiting the maximum current flowing through the PCB tracks. For the ADC, the analog supply and ground connections were routed separately to the regulator to limit noise coupling from other devices on the board. The IF outputs of the demodulator were routed with curved tracks, and surrounded with a ground plane to limit EMI. The assembled receiver board, attached to the generic USB interface is depicted in figure 4.

III. Software Environment

A graphical user interface (GUI) was written in C++ using Qt for Linux, for controlling the generic interface board. It is used to download the firmware to the CY7C68013A, writing the configuration file to the FPGA, allowing on-the-fly reconfiguration, as well as high-speed data reception. Buttons and sliders allow full control over the demodulation parameters of the TD1316 module. Coarse and fine gain can be modified, as well as the tuning frequency, channel spacing and automatic gain control (AGC) take-over point. At the same time, it is possible to retrieve data at high speed from the generic interface board through USB 2.0, for e.g. reception of streaming video data, apply software based error correction and decompression and show the video images or alternative information on the GUI screen. A I^2C slave implemented in the FPGA allows run-time control of the demodulation core parameters. A screen plot of the GUI for bit error rate measurements is depicted in figure 5.

IV. Case study : non-coherent FSK demodulation

As test case for assessing the receiver's functionality and performance, a FSK demodulation core was developed, compatible with previous work [4]. To demodulate digitized FSK data, the processing core has to discriminate between different frequencies, and quantize them into a stream of binary data. A robust method for demodulating FSK data is achieved by self-mixing a signal with a delayed version, followed by a low pass filter. This principle is applied in several analog demodulation ICs, and described in [14]–[16]. The self-mixing generates a 0 Hz and a double frequency component, with an amplitude proportional to the phase-shift. The double frequency is filtered out, leaving the 0 Hz component for further processing. In literature this is commonly described as FM-to-AM conversion or self-correlation, although a more self-explaining name is phase-shifted self-mixing (PSSM). The details of the improved PSSM are treated in a publication in progress [17].

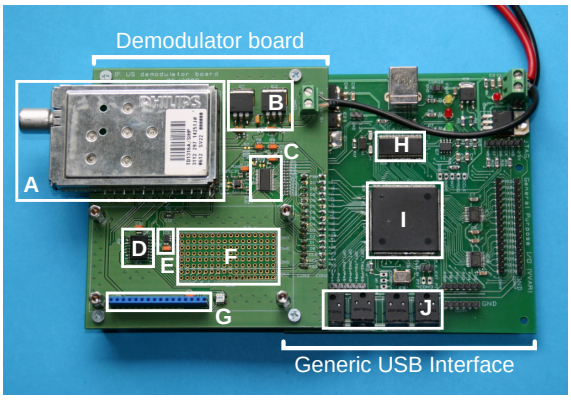


Fig. 4. PCB of the complete receiver and USB interface. Parts description: A. RF front end, B. voltage regulators, C. ADC, D. I^2C IO expander, E. I^2C DAC, F. patch area, G. LCD connector, H. Cypress USB interface IC, I. Xilinx FPGA, J. optical IOs

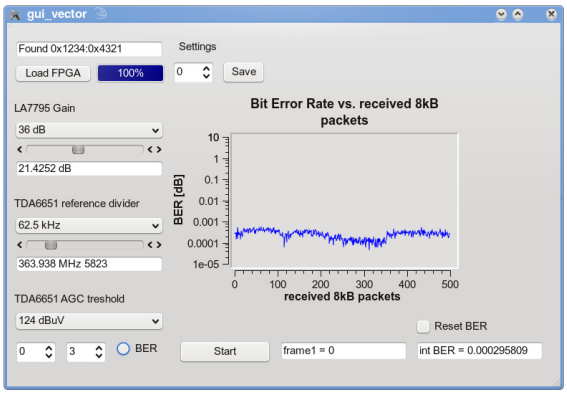


Fig. 5. Screen shot of the GUI developed in Qt for control of the receiver and real-time evaluation of the BER.

The PSSM approach was translated into a Matlab model and simulated, depicted in figure 6. The Matlab model was translated into VHDL, and functionally verified in Modelsim. The VHDL core was synthesized using Xilinx IDE and physically verified with an additional bit-error-rate (BER) testing core implemented in VHDL. A 32-bit linear-feedback shift register (LFSR) generates pseudo-random data at the input clock rate. This data output is controlling a TOSLINK optical transmitter, providing a galvanically isolated data input to modulate a wireless FSK transmitter. The wireless band is picked up by the reception antenna, and demodulated by the reconfigurable receiver. The demodulated data is compared to the transmitted data, counting the number of erroneously received bits. Every 64 kbit, the BER result is transmitted via USB to the PC GUI, and shown in realtime on the screen.

V. Conclusion and Future Work

A complete solution for wireless reception of any modulation scheme in the 50 to 800 MHz band has been developed. Complete reconfigurability is achieved by means of an FPGA, that can be reprogrammed on-the-fly. Received data can be transferred to a PC at high speed, using USB 2.0. Full control

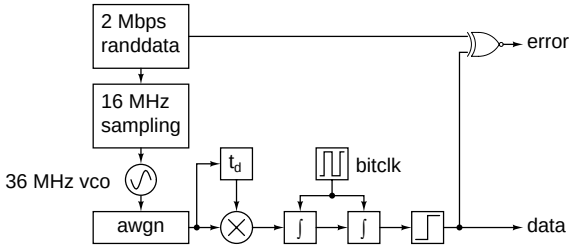


Fig. 6. Blockdiagram of the Matlab simulation of the PSSM algorithm.

over the demodulation parameters is enabled by I^2C control of the receiver front-end and its periphery. As test case, a FSK demodulation core was developed, implemented and tested in the receiver FPGA. Simulations and measurements suggest a performance better than the theoretical BER for non-coherent FSK reception [18].

The new receiver provides a flexible platform for performance measurements of newly developed transmitters, allowing fast exploration of the design space without the need for designing a dedicated receiver. This saves considerable time in the design cycle, allowing a faster time-to-market.

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